Si570 Clock Board V3.5 User's Guide

By Ian Jin & George Richardson Ver. 1.0

A. Features and Specifications

1. MCLK frequencies: 11.2896MHz, 12.2880MHz, 22.5792MHz, 24.5760MHz, 45.1584MHz, 49.1520 MHz, 90.3168 MHz, and 98.3040MHz (as built default)
2. MCLK ×Fs: 256×Fs, 512×Fs, 1024×Fs, 2048×Fs
3. Supported audio frequencies: 44.1KHz, 48KHz, 88.2KHz, 96KHz, 176.4KHz, 192KHz, 352.8KHz, and 384KHz
4. MCLK output: Two source terminated 50Ω u.fl output ports and one un-terminated u.fl output, LVTTL level
5. Working mode: FIFO mode and standalone mode
6. Inverted MCLK: Enabled as default (see text below for explanation)
7. External Controller: Supported via UART
8. Automatic Fs switching function: Supported in FIFO mode, Frequency/×Fs combination strategy is manually settable. An external, third-party controller can be used as a controller
9. Dual-mono DAC support: Native
10. I^2S re-clocking: Included
11. Power Requirement: 4V-6V DC @ 150mA. Power may be supplied from the FIFO or from an external DC source
12. Si570 Published Performance:[*]

Phase noise (dBc/Hz)

100Hz	-112
1KHz	-122
10KHz	-132
1MHz	-137
10MHz	-150

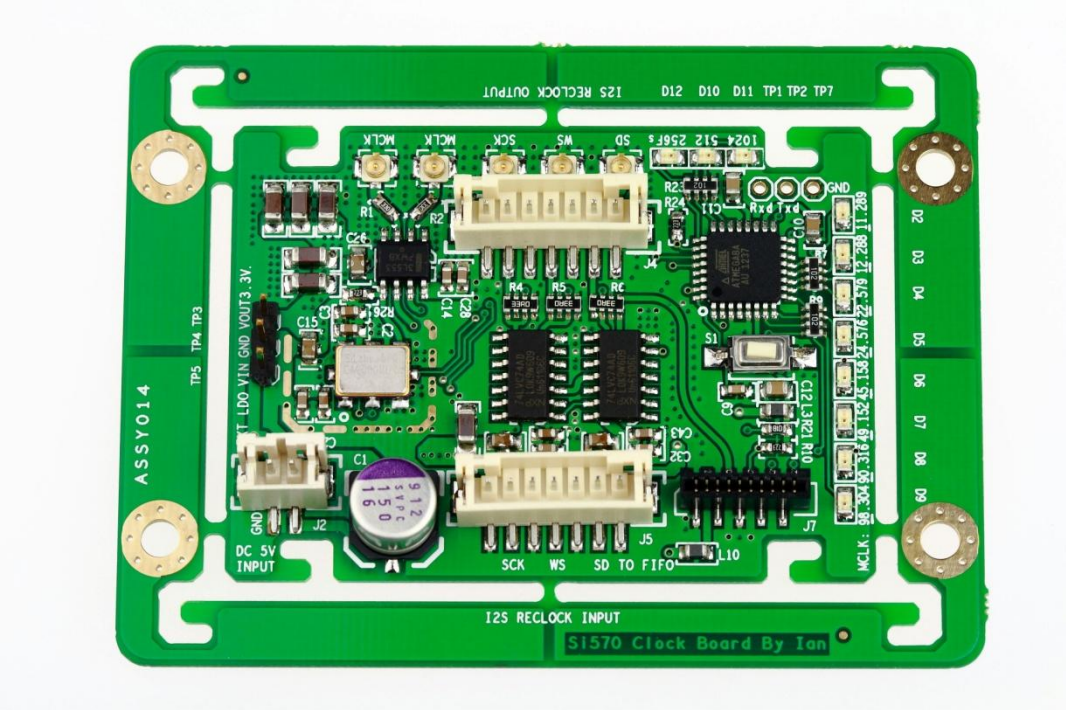
Period Jitter: 2ps RMS, 14ps Peak-to-Peak

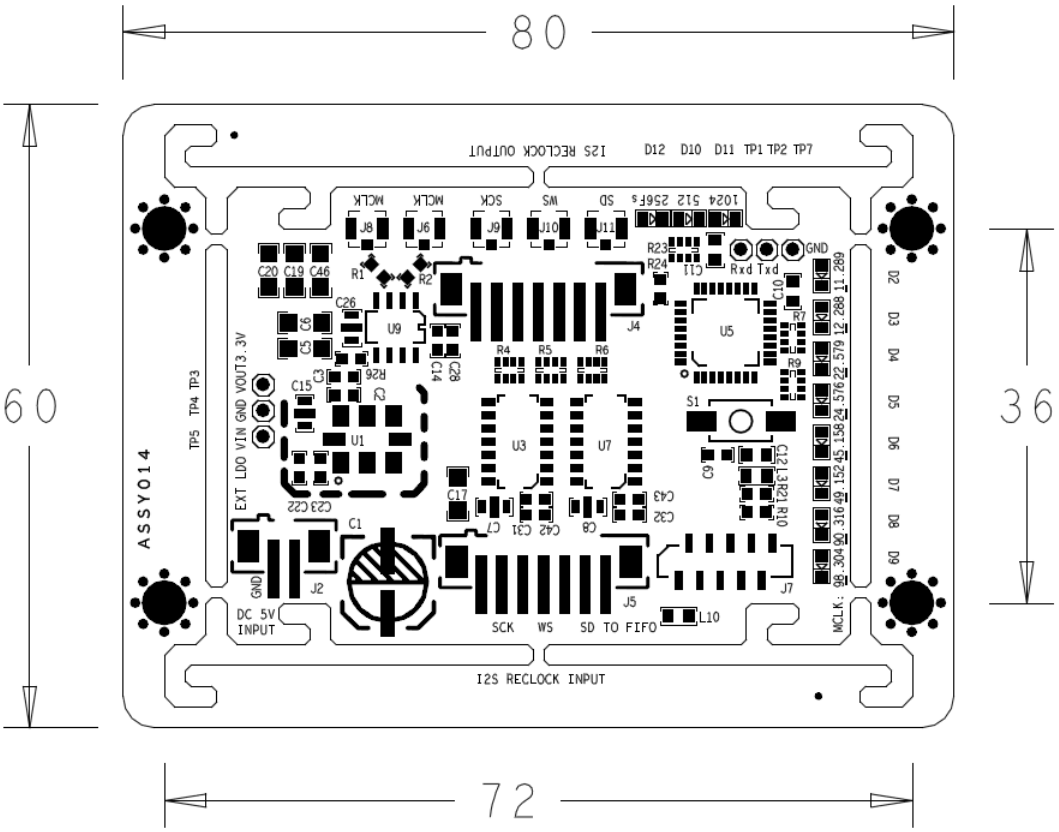
Frequency Stability: ±50ppm

[*] From Si570 datasheet. Available at www.silabs.com.

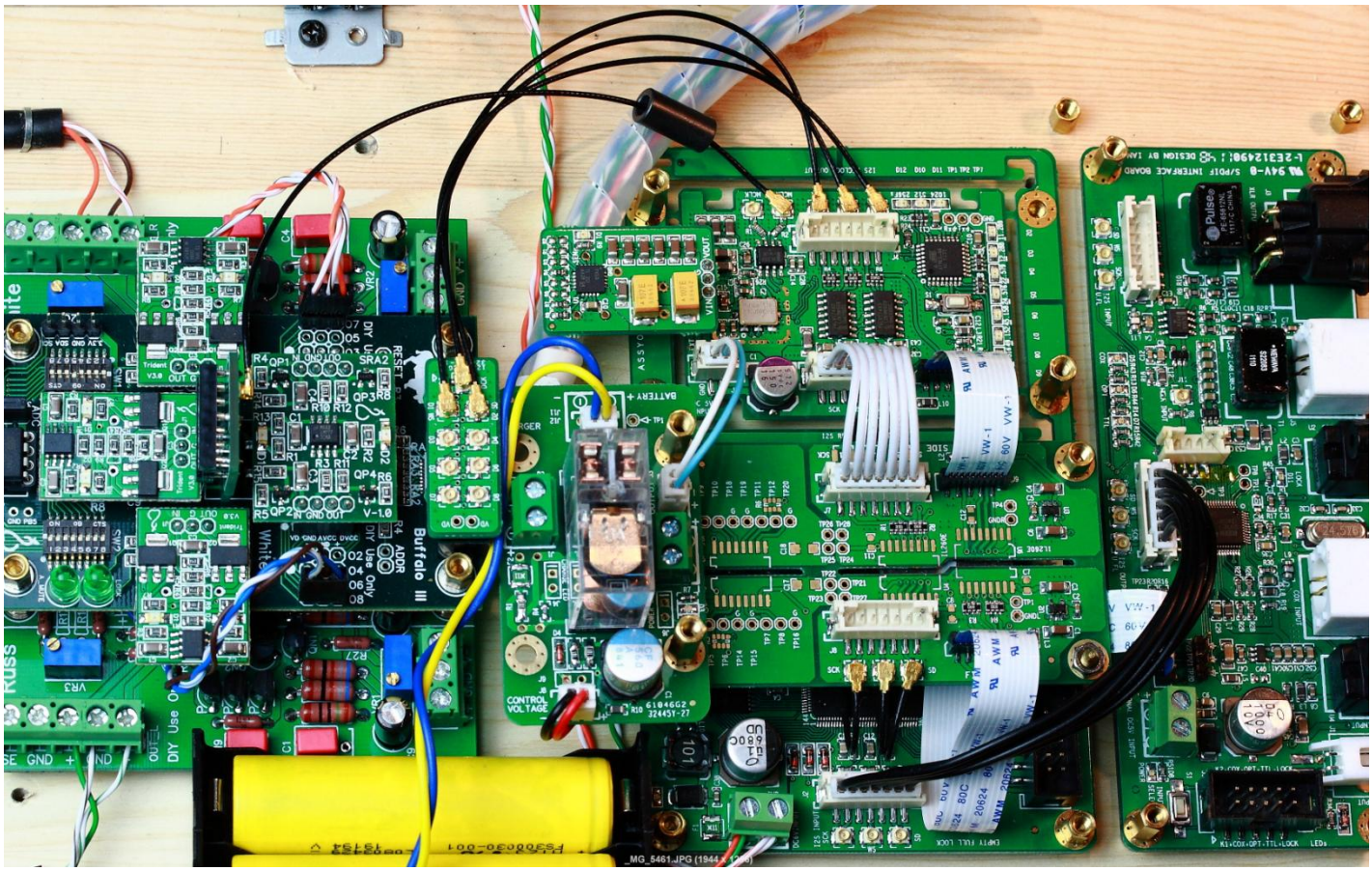
[†] I^2S signal names are based on the Philips standard. Other nomenclature may be used, e.g., BCK = SCK; LRCK = WS; DATA = SD.

B. Layout and Dimensions (in mm)

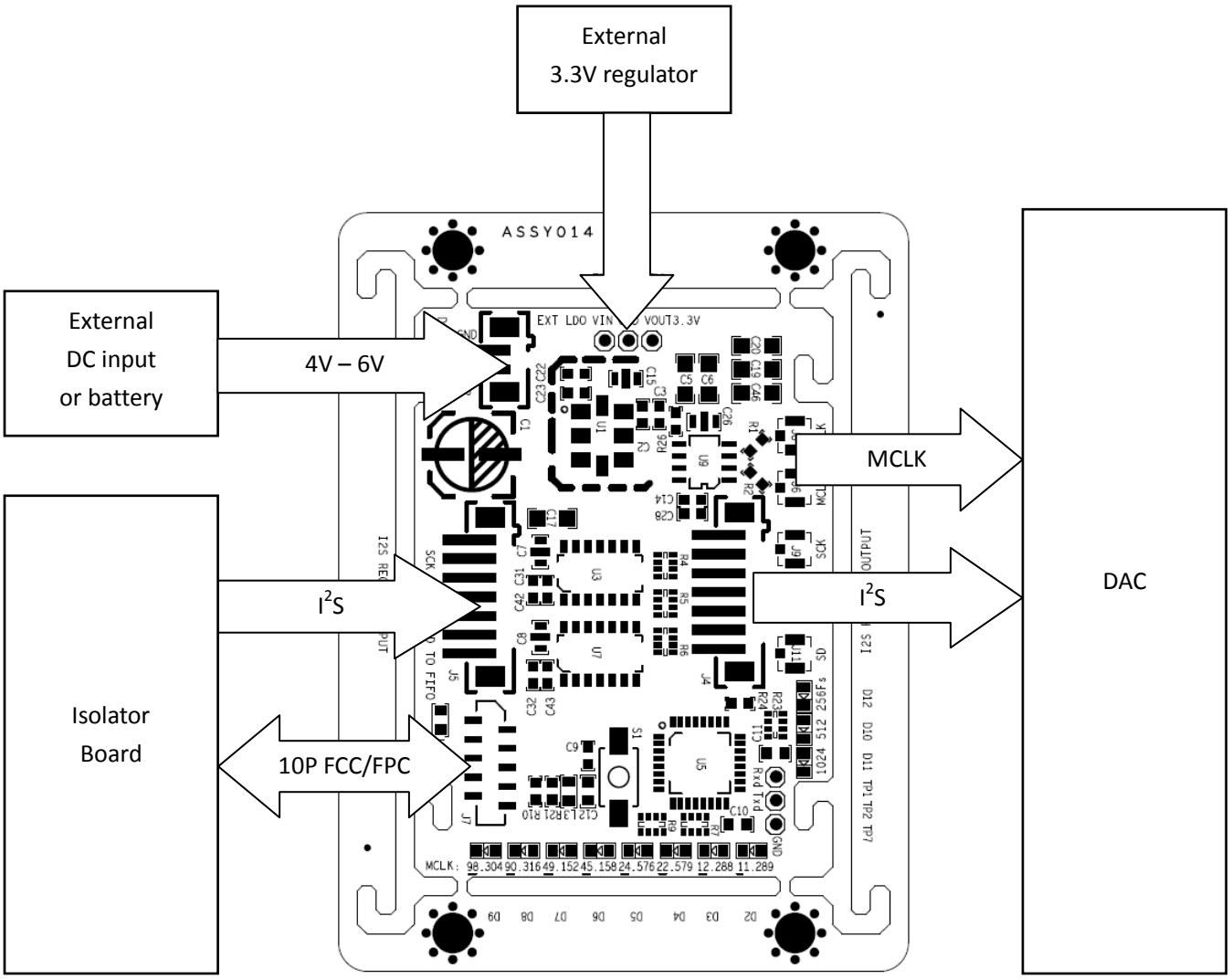




C. Typical System Configuration

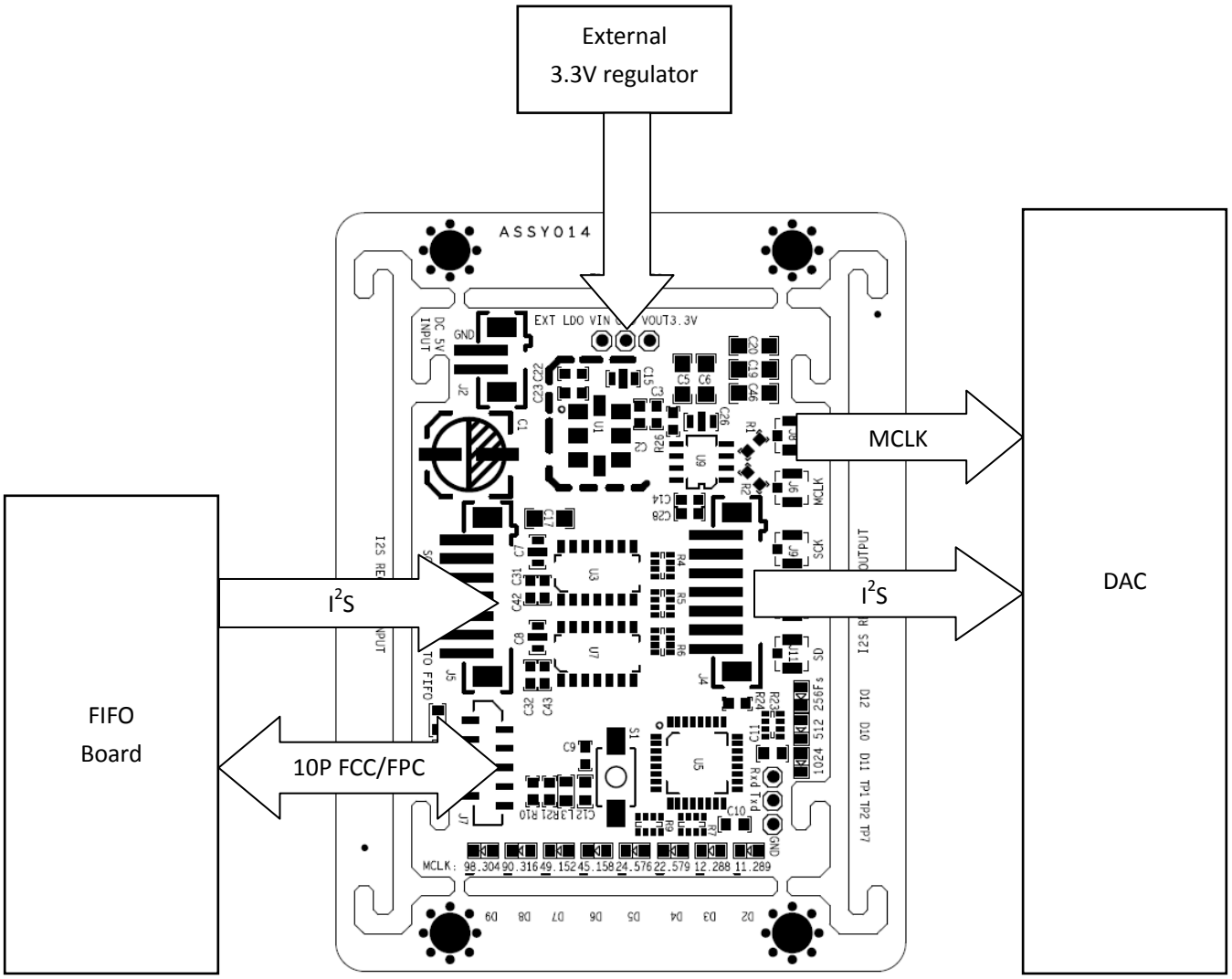


D. Using the Si570 Clock Board with a FIFO and Isolator Board (recommended)



This is the recommended, "full feature" configuration. The Si570 Clock Board is isolated from the I^2S source and FIFO by the isolator board (available separately). This isolation requires the Si570 Clock Board to have its own power source. Appropriate power sources are discussed below. Depending on the power source, the Si570 Clock Board may need an external 3.3V regulator. Appropriate regulators are discussed below.

E. Using the Si570 Clock Board with a FIFO without the Isolator Board



In this configuration, the Si570 Clock Board is used without an isolator board. The Si570 is connected directly to the FIFO board by a 10P FFC/FPC cable and obtains its power from the FIFO board. In this configuration, the Si570 Clock Board requires an external 3.3V regulator. Appropriate regulators are discussed below.

F. Using the Si570 Clock Board in Standalone Mode

The Si570 Clock Board can be used by itself as a universal digital audio clock generator. In this standalone mode, the Si570 Clock Board must have its own power source. Appropriate power sources are discussed below. Depending on the power source, the Si570 Clock Board may need an external 3.3V regulator. Appropriate regulators are discussed below. In the standalone mode, the output frequency can be selected manually at any time by using the on-board push button, S1. See "Manually Setting Frequencies," below. The selected frequency is stored onboard in flash memory and will be recalled automatically on each power up.

G. Connectors and Indicators

Connector	Description	Notes	Type	Comments
MCLK	Two MCLK outputs; 50Ω U.FL	The 2 outputs are equivalent in function but come from different drivers; either output can be used for stereo DACs; use both for dual-mono DACs (Do not connect to S/PDIF board)	U.FL	required for DACs in sync mode
J5	I^2S input for re-clocking 2 – SCK 4 – WS 6 – SD 1,3,5,7 – GND	Connects to I^2S source on isolator board, FIFO board, or other I^2S source	7P PH2.0mm	recommended
SCK, WS, SD†	I^2S re-clocked output; 50Ω U.FL	Connects to I^2S input of DAC; equivalent function to J4 with better signal integrity	U.FL	recommended
J12, J13, J14	Optional I^2S re-clocked output; 50Ω U.FL	Second group of I^2S output for dual-mono DACs; equivalent function to above I^2S output with individual source terminating resistors, U.FL sockets need to be added	U.FL	optional
J2	DC input 1 – GND 2 – DC 4V – 6V	Used to connect external DC power source when used with an isolator board or in standalone mode; must be left open if used with FIFO directly without an isolator board	2P PH2.0mm	conditional
TP3, TP4, TP5	External 3.3V regulator TP5 – V_{IN} TP4 – GND TP3 - V_{OUT}	Connection for external 3.3V regulator; See “Powering the Si570 Clock Board,” below	SIP3 2.54mm	usually required
J7	Control cable	Connects to isolator board or FIFO board	10P FPC	required except as standalone
S1	Push button to manually set frequency or frequency/×Fs combination	See “Manually Setting Frequencies,” below	Push button	

† I^2S signal names are based on the Philips standard. Other nomenclature may be used, e.g., BCK = SCK; LRCK = WS; DATA = SD.

Connector	Description	Notes	Type	Comments
TP1, TP2, TP7	External controller TP1 - Rxd TP2 – Txd TP7 – GND	UART port for optional external controller See “Using an External Controller,” below	SIP3 2.54mm	Optional
J1	Optional MCLK	Optional un-terminated MCLK output; U.FL socket needs to be added for use; cable has to be very short or be terminated at device end	U.FL	Not recommended
J15, J16, J17	Optional I^2S input for re-clocking 2 – SCK 4 – WS 6 – SD 1,3,5,7 – GND	Alternative to J5, equivalent in function; U.FL sockets need to be added to use	U.FL	Optional
J4	Optional I^2S re-clocked output 2 – SCK 4 – WS 6 – SD 1,3,5,7 – GND	Alternative to I^2S output via U.FL, equivalent in function	7P PH2.0mm	Optional Use I^2S output via U.FL if possible
D2 – D9	MCLK indicators	Indicates the current MCLK frequency 11.2896MHz, 12.2880MHz, 22.5792MHz, 24.5760MHz, 45.1584MHz, 49.1520 MHz, 90.3168 MHz, or 98.3040MHz	8 LEDs	
D10 – D12	×Fs indicators	Indicates the current ×Fs 256×Fs, 512×Fs, 1024×Fs, 2048×Fs (All on)	3 LEDs	

H. Powering the Si570 Clock Board

The way in which the Si570 Clock Board is powered depends on the configuration. When used with a FIFO board but without an isolator board, the Si570 Clock Board draws its power from the FIFO board via the 10P FFC/FPC cable connected to J7. When used with an isolator board, the Si570 Clock Board requires its own power source. There are two ways to power the Si570 Clock Board:

1, Using the Si570 Clock Board with the FIFO and an isolator board (recommended)

This is the best way to run the Si570 Clock Board and ensures the lowest EMI noise by cutting the ground loop. In this case, the Si570 Clock Board must be powered from an external power source connected to DC input J2. Please note that in this configuration, half of the isolator board will be powered from the same DC power source as the Si570 Clock Board.

2, Using the Si570 Clock Board with the FIFO without an isolator board

In this case, the Si570 Clock Board is powered automatically from the 10P FFC/FPC cable connected to the FIFO. Leave the DC input connector, J2, unconnected, otherwise the two DC supplies will short. L10 on the Si570 Clock Board may be removed, but this is not recommended.

3, Using the Si570 Clock Board as a standalone audio clock generator without connecting to a FIFO

In this case, the Si570 Clock Board must use an external power source connected to DC input J2 (i.e., the same as the first case).

I. External Regulator Solutions

When using a power source other than a 3.2V $LiFePO_4$ battery cell (discussed below) an external 3.3V regulator must be connected to TP3, TP4, and TP5 on the Si570 Clock Board. The external regulator will significantly change the sound quality of the Si570 Clock Board. Careful selection of this regulator is required according to personal preference. Please note generally that, when choosing a regulator, a regulator that performs well in an audio amplifier may not be a good candidate to power an oscillator. A good oscillator power supply needs not only very low noise, but also must maintain that performance in high-frequency RF/VCO applications. Some of the possible regulator solutions are:

1, TPS7A4700 low-noise LDO board (recommended)

This LDO board has been determined to be one of the best ways so far to power the Si570 Clock Board. Although the LDO board can plug into the 3P SIP socket, it is preferable to solder it directly to the pins once you have determined to use it permanently. The TPS7A4700 regulator board can be placed either vertically or horizontally on the Si570 Clock Board.

The six output capacitors on the right side of the LDO board affect the sound of the Si570 Clock Board significantly. Changes and improvements can be made with different capacitors. See “Tips for Further Improvement,” below.

2, Third-party 3-pin “discrete” regulator boards

Many candidates are available, but be sure that the output current is sufficient to power the Si570 Clock Board, which requires 150mA.

3, Shunt regulators

Any 3.3V shunt regulator may work, but the high-frequency performance has to be confirmed to be suitable to power an oscillator.

4, Standard TO220-3 3.3V IC

A standard 3-pin LDO, such as an A78M33, will work and is pin-to-pin compatible with TP3, TP4, and TP5. This is not recommended, however, because of poor noise performance. The datasheet for the TI uA78M33, for example, indicates that the regulator may have as much as 200µV of noise.

5, Direct 3.2V $LiFePO_4$ battery cell

To use direct battery power, the Si570 Clock Board must be used with an isolator board (or in standalone mode). To use a battery:

(1) Short TP5 (V_{IN}) and TP3 (V_{OUT}) with a jumper

(2) Connect a 3.2V $LiFePO_4$ battery (i.e., a single cell or multiple cells **in parallel**) using the battery management board (available separately) to DC input connector J2.

When using an isolator board, half of the isolator board will be powered by the same 3.2V battery automatically via the 10P FFC/FPC cable on J7. Ordinarily it is not necessary to remove or bypass the LDO on the isolator board because most of the LDOs tested were able to power half of the isolator with a 3.2V input (although the LDO output will be a bit lower than 3.2V).

J. Manually Setting Frequencies

When the Si570 Clock Board is used in the standalone mode, the output frequency can be set manually by using the on-board push-button, S1. The selected frequency will be stored in the onboard flash memory and will be recalled automatically upon power up.

To set a desired output frequency:

1, Press and hold the on-board push button, S1.

2, After about two seconds, the frequency LED indicators, D2-D9, will start flashing and then light sequentially.

3, Release S1 at the moment the LED indicating the desired frequency is lit.

4, That LED will flash a few times and then become solid, indicating that the new frequency has been set successfully.

K. Automatic Fs Switching and Frequency/×Fs Combination Groups

When used with a FIFO, frequencies and ×Fs will be switched automatically according to the input I^2S Fs and the preset frequency and the ×Fs combination group. The four pre-set combination groups are:

//Group1: Si570 frequency and ×Fs combination for low MCLK range

{F112896, 256×FS} 44.1 KHz

{F122880, 256×FS} 48 KHz

{F225792, 256×FS} 88.2 KHz

{F245760, 256×FS} 96 KHz

{F451584, 256×FS} 176.4KHz

{F491520, 256×FS} 192 KHz

{F903168, 256×FS} 352.8KHz

{F983040, 256×FS} 384 KHz

// Group2: Si570 frequency and ×Fs combination for low to mid MCLK range

{F225792, 512×FS} 44.1 KHz

{F245760, 512×FS} 48 KHz

{F225792, 256×FS} 88.2 KHz

{F245760, 256×FS} 96 KHz

{F451584, 256×FS} 176.4KHz

{F491520, 256×FS} 192 KHz

{F903168, 256×FS} 352.8KHz

{F983040, 256×FS} 384 KHz

// Group3: Si570 frequency and ×Fs combination for middle MCLK range

{F451584, 1024×FS} 44.1 KHz

{F491520, 1024×FS} 48 KHz

{F451584, 512×FS} 88.2 KHz

{F491520, 512×FS} 96 KHz

{F451584, 256×FS} 176.4KHz

{F491520, 256×FS} 192 KHz

{F903168, 256×FS} 352.8KHz

{F983040, 256×FS} 384 KHz

// Group4: Si570 frequency and ×Fs combination for high MCLK (default)

{F903168, 2048×FS} 44.1 KHz

{F983040, 2048×FS} 48 KHz

{F903168, 1024×FS} 88.2 KHz

{F983040, 1024×FS} 96 KHz

{F903168, 512×FS} 176.4KHz

{F983040, 512×FS} 192 KHz

{F903168, 256×FS} 352.8KHz

{F983040, 256×FS} 384 KHz

Group4 is highly recommended for use with ESS DACs.

The default combination groups can be programmed by using the on-board push button and will be saved in the on-board flash memory.

To program group1 as the default combination, manually set the frequency to 12.2880MHz or 11.2896MHz;

To program group2 as the default combination, manually set the frequency to 24.5760MHz or 22.5792MHz;

To program group3 as the default combination, manually set the frequency to 49.1520MHz or 45.1584MHz;

To program group4 as the default combination, manually set the frequency to 98.3040MHz or 90.3168MHz;

L. Inverted MCLK Function

The inverted MCLK function is enabled as the default setting. This feature is designed to optimize the noise performance in the synchronous mode according to the application note for the ESS DAC. With this function, the rising edge of the MCLK pulse will be a half period prior to the changing on I^2S signals. Listening tests revealed that using the inverted MCLK function had a noticeable positive effect on the sound. This feature may have a similar positive effect on other DACs.

To disable the inverted MCLK function,

1, Remove U2 and

2, Short R28 with a 0Ω 0603 jumper.

M. Using an External Controller (optional for high level user)

The Si570 driver makes available its status display and part of its frequency control to an external controller via a UART. The UART connection is reserved on the board as TP1, TP2, and TP7. A UART isolator is recommended when using an external controller.

The communication protocol for an external controller is:

//Si570 multi-frequency clock board serial communication protocol V1.0 2012-11-03 by Ian

//UART 9600,n,8,1

//events sent from si570 driver

//Format: 0xAA,EVENT,DATA,0x55

//EVENTS:

#define GETNEWFS 0xC1 //FIFO detected a new Fs which need a new MCLK frequency

#define SETFRQ 0xC2 //new Si570 frequency is set

#define SETXFS 0xC3 //new xfs is set

#define WRONGINPUTCMD 0xC4 //wrong input command or no input command

#define WRONGINPUTFRQ 0xC5 //input frequency is overange

```
#define INVALIDINPUTFRQ       0xC6    //input frequency is invalid for current Fs
//Command response from external controller
//Format: 0xA5,CMD,DATA,0x5A
//0xC8 command has to be sent within 100ms after getting event 0xC1,
//otherwise the Si570 driver will set the frequency and ×Fs according to the preset without stopping the music
//CMD:
#define TOINPUTFRQ          0xC8    //set frequency for the new detected Fs by external controller
//sample frequency data of event 0xC1,
//#define FS22          0
//#define FS24          1
//#define FS44          2
//#define FS48          3
//#define FS88          4
//#define FS96          5
//#define FS174         6
//#define FS192         7
//#define FS352         8
//#define FS384         9
//xfs data for event 0xC3
//#define XFS256        0
//#define XFS512        1
//#define XFS1024       2
//#define XFS2048       3
//frequency data for event 0xC2 and command 0xC8
//#define F112896       0
//#define F122880       1
//#define F225792       2
//#define F245760       3
//#define F451584       4
//#define F491520       5
//#define F903168       6
```

//#define F983040 7

N. Driving a Dual-Mono DAC

The Si570 Clock Board was designed natively to support DACs operating in a dual-mono configuration.

For a dual-mono DAC, it is highly recommended that the two sets of signals are connected to the DAC with 50Ω coaxial cables, because proper impedance matching is important to reduce SWR. Moreover, the cables must be of the same length so that both sets of signals arrive at same moment. This is because every 25mm of cable causes a delay of roughly 120ps! (assuming the cable's velocity of propagation is .7C). In this case, U.FL sockets for the second group of I^2S output have to be mounted on the bottom side of the PCB using the footprints of J12, J13, and J14.

O. Application Notes

1. The Si570 Clock Board has been optimized for digital audio applications that require a high frequency MCLK up to 98.3040MHz, as well as a multi-frequency output capability. The Si570 Clock Board may not be the best choice if all that is needed is a low frequency MCLK, for example, 22.5792MHz or 24.5760MHz.

2. The Si570 Clock Board operates in the double speed mode natively. It is not recommended to feed its MCLK into the DIT section of the S/PDIF board as part of a S/PDIF FIFO (can work with S/PDIF DIR without problem). If necessary, the MCLK from the FIFO board may be fed to the S/PDIF Interface board MCLK U.FL socket.

3. The Si570 device is a crystal-based programmable oscillator which uses a high Q crystal inside a metal case. When used for the first time, the Si570 needs a few hours to burn in before it becomes stable. Thereafter, only a few minutes warm up time are needed at each power up.

4. The power supply significantly affects the sound quality and style of the Si570 Clock Board. Careful selection and tuning of the power supply is important to achieve the best performance according to personal preference. Please see the related tips below for suggestions.

5. The Si570 Clock Board is set to 98.3040MHz and combination group 4 as a default. As built, it can be connected immediately to an ESS DAC in either the SYNC/ASYNC mode and either stereo or dual-mono configurations. Other DACs may require a different MCLK frequency or combination group, in which case set the MCLK frequency and the ×Fs combination group manually according to the particular DAC's specifications at first time of running.

6. Please note that different MCLK/×Fs combination groups may sound different even when playing the same I^2S track.

P. Tips for Further Improvements

1. The Si570 Clock Board's power supply determines the sound quality. Choosing a good external regulator is important to achieve the best performance.

2. The output capacitors on the TPS7A4700 LDO board affect the sound quality significantly. The output capacitors included on the finished TPS7A4700 LDO board are 10µF 25V multilayer ceramic capacitors ("MLCC") with an X7R temperature profile. They produce a sound with great detail, quiet background, and beautiful trebles. But another brand of 10µF MLCC was tried and it produced a wonderful mid-range. Thus, it is suggested that different capacitors be tried to find the sound that appeals most to you.

3. The DC input also is very important. Ultra low-noise power is preferred. Battery-based 4V-6V DC power in conjunction with the passive management board is recommended as a simple way to get good results.

4. Try good optional output capacitors on the bottom side of the PCB in positions C4, C16, C40, C41, and C44. The footprint is 1206, which will fit MLCC or A-size tantalum capacitors. Positions C36 and C39 will fit E-size tantalum capacitors or bigger package MLCCs. Multilayer ceramics should have a temperature profile of X7R or better. Bear in mind, however, that the output capacitor is an integral part of the external LDO's feed-back loop. Thus, if you change output capacitors, you must ensure that the LDO will operate properly with a larger capacitive load.

5. Try optional input capacitors on the bottom side of the PCB in position C38. The footprint will accept E-size tantalums or suitably sized MLCCs.

6. The Si570 Clock Board is supplied with flip-flops from NXP. The NXP devices were chosen in part because of the reliability of a well-established, large manufacturer, as well as excellent actual evaluation and measurement result. You can replace the NXP flip-flops with the Potato Semiconductor PO74G74. They are available on eBay and at potatosemi.com. The 74G74 is tested to have 0.2ns less Tpd than the NXP device. Based on test results, both devices have very good re-clocking performance. The ESS DAC locks perfectly on either device at the lowest bandwidth without any issues. Listening tests did not reveal a difference in sound quality between the two, but maybe you will hear a difference. If you use the 74G74 in a dual-mono DAC configuration, you must ensure that the 74G74 has sufficient drive current to maintain a good rise/fall time and logic level.

7. A metal shield over the Si570 chip could reduce EMI noise.

8. Rubber suspensions are recommended to isolate the board from mechanical vibration, which can cause piezoelectric effects on both the Si570 crystal and the MLCCs.

Q. Period Jitter Measurements of the Si570 Clock Board in the Time Domain

1. Jitter measurement results

   Period jitter (RMS): 3.85ps

   Period jitter peak-to-peak: ±12ps

   Jitter distribution: Gaussian

   Frequency: 98.3097MHz

2. Test conditions

Test equipment: LeCroy LC584AXL with JTA package

Jitter measurement noise floor: 2ps

Number of Samples: N=10,000 cycle

Sampling rate: 8 GSa/s

3. Some notes

This test results are just for reference. Different Si570 chips may have slightly different jitter performance. Measuring the clock period jitter in the time domain is the easiest way to evaluate a clock, but it may not be the best method. The best way to analyze the jitter of a clock is to measure the phase noise in the frequency domain using a signal source analyzer. A phase noise plot can reveal more details by spectrum.