Analog Reinvented

ES9033

32-bit High-Performance 2-Channel DAC with line drivers

Product Brief

The Sabre ES9033 High Performance Audio DAC is a 32-Bit, 2-channel audio DAC that brings professional, digital audio quality to the consumer home entertainment market.

Using ESS' patented HyperStream® II architecture, the Sabre ES9033 delivers studio quality audio with 122dB DNR (w / DRE) and –108dB THD+N.

With the integrated line drivers, the ES9033 reduces BOM costs by eliminating the need for external amplifier to produce a line level $2V_{rms}$ output.

The Sabre ES9033 flexible input architecture accepts up to serial 32 bit serial PCM data to 768kHz sample rate & DSD512.

The Sabre DAC sets a new standard for high-quality audio performance in a cost-effective, compact, easy to use form factor for today's most demanding digital audio applications.

FEATURE	DESCRIPTION
+122dB (w/ DRE) DNR per channel -108dB THD+N per channel	Unprecedented dynamic range and ultra-low distortion
High Sample Rates	Support for up to PCM 768kHz & DSD512
2-channel DAC + Line Driver in 28-QFN	Reduced footprint and simplifies board layout
Multiple formats available	PCM, TDM, DSD, DoP input data formats
Customizable filter characteristics	8 preset filters
I2C, SPI, and Hardware interface control	Configured by microcontroller or other I2C/SPI source, or pins through Hardware Mode
Integrated low noise DAC reference regulators	Reduced BOM cost, PCB area and improved DNR.
Low Pin Count standardized Packaging	5mm x 5mm, 28 pin QFN
2Vrms Integrated Line Driver	Reduces BOM costs w/o required external opamp required for line driver levels
Analog PLL (APLL)	Simplifies clocking requirements and reduces PCB size and BOM cost

APPLICATIONS

- Media Streamer Applications
- Gaming Motherboards
- Audio Receivers
- Professional Audio Equipment
- Active Speakers

Functional Block Diagram

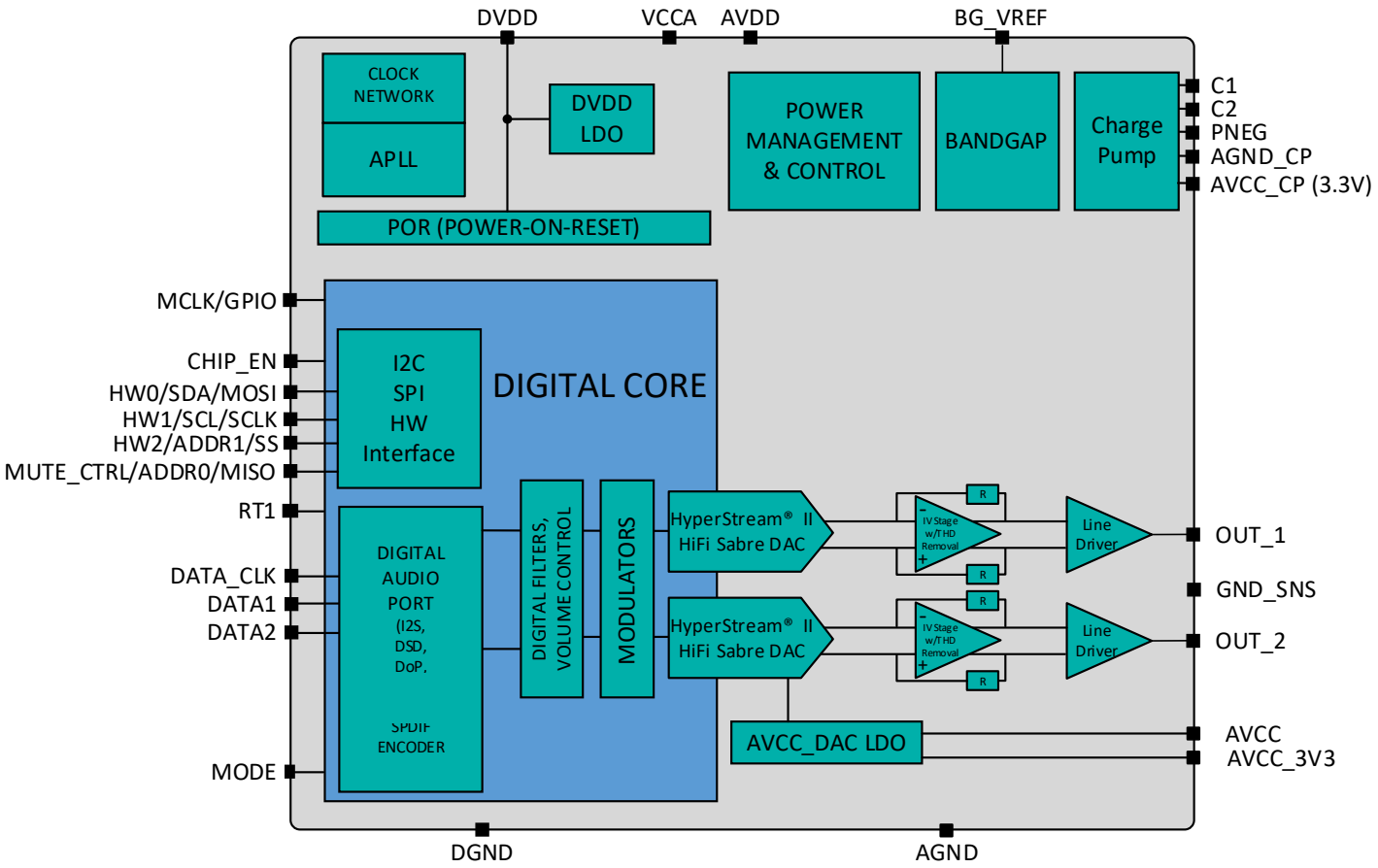
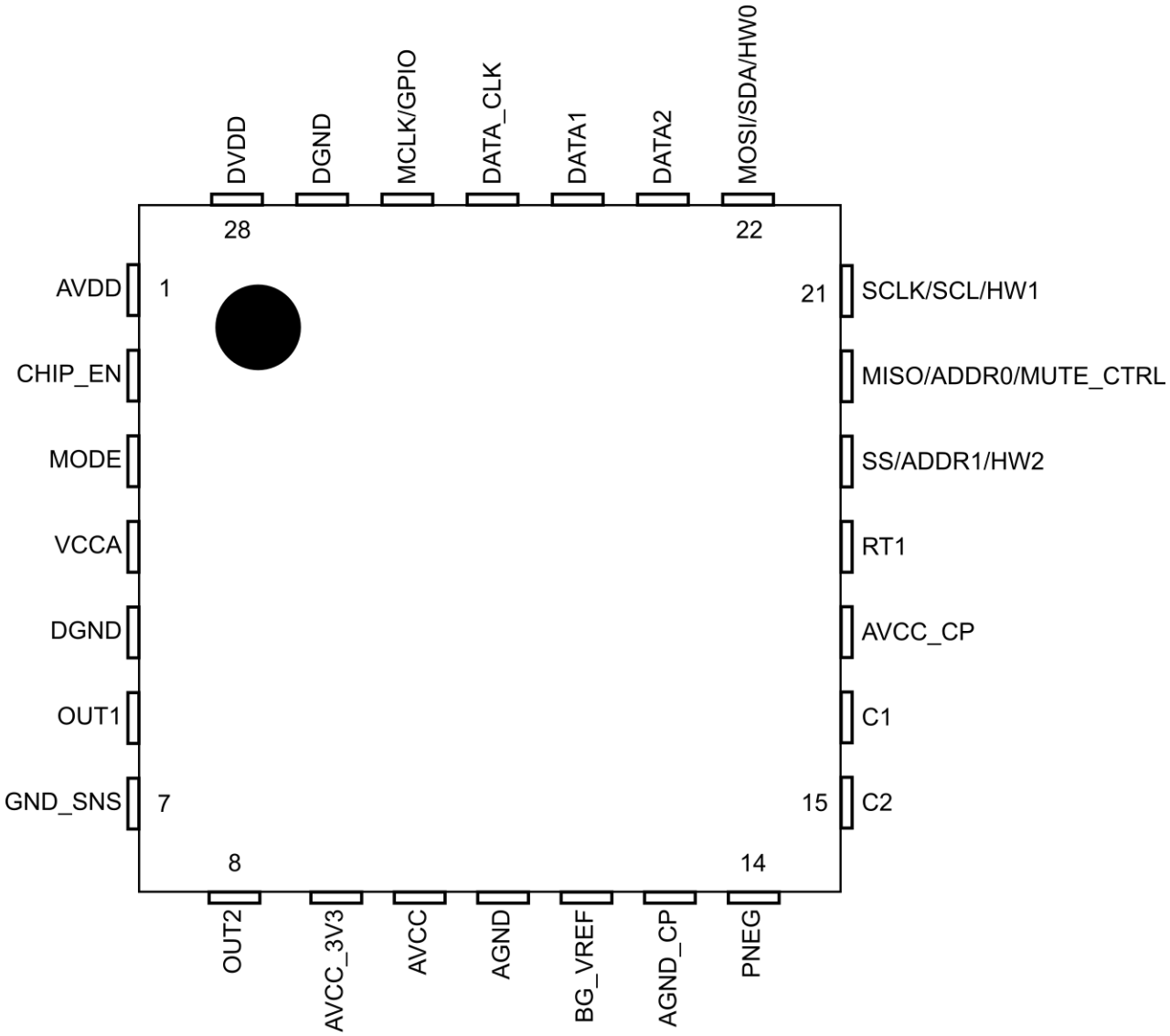


Figure 1. ES9033 Block Diagram

ES9033 28 QFN Pinout



ES9033Q
(Top View)

28 QFN Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	AVDD	Power	Power	3.3V or 1.8V I/O supply
2	CHIP_EN	I/O	HiZ	Active-high chip enable.
3	MODE	I/O	HiZ	Control for SPI/I2C/HW modes
4	VCCA	Power	Power	Analog Supply
5	DGND	Ground	Ground	Digital ground
6	OUT1	AO	Ground	Output channel 1
7	GND_SNS	AI	Ground	Line driver load ground voltage sense
8	OUT2	AO	Ground	Output channel 2
9	AVCC_3V3	Power	Power	Analog Regulator 3.3V Supply
10	AVCC	Power	Power	Analog Regulator Output, internally supplied
11	AGND	Ground	Ground	Analog ground
12	BG_VREF	AO	Ground	Bandgap Voltage reference
13	AGND_CP	Ground	Ground	Analog Ground for charge pump
14	PNEG	Power	Ground	Integrated chargepump output. Line driver negative supply.
15	C2	-	-	Line driver negative flying capacitor
16	C1	-	-	Line driver positive flying capacitor
17	AVCC_CP	Power	Power	Analog Supply for charge Pump
18	RT1	I	HiZ	Reserved. **Must be connected to DGND for normal operation**.
19	SS/ADDR1/HW2	I/O	HiZ	Interface Signal (SPI/I2C/Hardware modes)
20	MISO/ADDR0/MUTE_CTRL	I/O	HiZ	Interface Signal (SPI/I2C/Hardware modes)
21	SCLK/SCL/HW1	I/O	HiZ	Interface Signal (SPI/I2C/Hardware modes)
22	MOSI/SDA/HW0	I/O	HiZ	Interface Signal (SPI/I2C/Hardware modes)
23	DATA2	I/O	HiZ	Serial DATA2
24	DATA1	I/O	HiZ	Serial DATA1
25	DATA_CLK	I	HiZ	Serial data clock
26	MCLK/GPIO	I/O	HiZ	MCLK input, General I/O
27	DGND	Ground	Ground	Digital core ground
28	DVDD	Power	Power	Digital core supply, internally supplied
29*	Package PAD	-	-	Not electrically connected, used for heat dissipation

* Note: Pin 29 is the package pad.

Ordering Information

Part Number	Description	Package
ES9033Q	SABRE 32-bit 2 Channel DAC with built in line driver & digital filters	5mm x 5mm 28 QFN
ES9033TQ	SABRE 32-bit 2 Channel DAC with built in line driver & digital filters Extended temperature range -40 to 125deg Celsius	5mm x 5mm 28 QFN

Revision History

Current Version 0.2.3

Rev.	Date	Notes
0.2	February 12, 2021	Initial release
0.2.1	March 19, 2021	Pin 5 description change
0.2.2	April 1, 2021	Added ES9033TQ to ordering information, changes to wording
0.2.3	April 5, 2021	Updated last page, updated pinout diagram for clarity